Horizontal convergence data from the red RAM (U46) are input to latches U50 and U51. The output of U50 feeds multiplying DAC U53. Similarily, the output of U51 feeds DAC U52. Each DAC contains a transparent latch. Both DACs are loaded with new data every horizontal time slot in the following manner:

Consider a time slot divided into 4 equal parts - 1/4, 2/4, 3/4 and 4/4. During 1/4, a convergence value for the zone containing the current scan line is clocked into latch U50 on the rising edge of HCLKA. During 2/4, the convergence value for the next zone is clocked into latch U51 on the rising edge of HCLKB. During 3/4 and 4/4, the write-enable pulse HCLK* is driven low. The bytes in the two latches are simultaneously loaded into the DACs on the rising edge of HCLK* at the end of the 4/4 interval. Clock signals HCLK*, HCLKA and HCLKB are generated by U45.

By using the waveforms H-ALPHA and H-ALPHA-I from the "alpha" circuit, the two DACs solve the interpolation equation,

$$C = (I/N) * A + (1-I/N) * B,$$

where 'C' is the final output voltage, 'A' is the convergence value in one DAC, and 'B' is the value in the other DAC. The 'I/N' and '1-I/N' terms are represented by H-ALPHA and H-ALPHA-I, respectively. The data in U53 (A) is multiplied by H-ALPHA, which is input as the DAC's reference voltage. The data in U52 (B) is similarily multiplied by H-ALPHA-I. The resulting voltages are summed together in U400. H-ALPHA-REF is also added to ensure a bipolar output.

A smooth interpolation between the 'A' value at the start of a zone and the 'B' value at the start of the next zone occurs because H-ALPHA and H-ALPHA-I are complementary waveforms. At the start of a zone, one voltage is full scale, while the other is zero. The full-scale voltage ramps linearly down to zero, decreasing by a small increment on each scan line. The other voltage ramps up to full scale in a similar manner, so that by the end of the zone, the voltage levels have reversed.

To reduce the effects of gain and offset errors in the DACs, the 'A' and 'B' values alternate between the two DACs every zone. On even zones, 'A' is loaded into U53 and 'B' is loaded into U52. On odd zones, 'A' is loaded into U52 while 'B' is loaded into U53. This ensures that a new value is loaded into a DAC only when its reference voltage is zero, eliminating the possibility of an abrupt voltage change or "basketweave" artifact.

DACs U47 and U48 create the red vertical convergence waveform in a similar manner, using V-ALPHA, V-ALPHA-I and V-ALPHA-REF, and timing signals VCLKA, VCLKB, and VCLK*. Vertical convergence values are clocked into latches U47 and U48 during intervals 3/4 and 4/4, respectively. The data are then clocked into the DACs at the end of the 2/4 interval.

The green and blue waveform channels are similar to the red waveform channels. To support "global" and zonal geometry corrections, the green vertical waveform (GV) is added to both the red and blue vertical waveforms. Similarly, the green horizontal waveform (GH) is added to the red and blue horizontal waveforms. Horizontal rate parabolas generated in software are loaded into the vertical half of the green RAM to allow user adjustment of top pincushion, bottom pincushion and bow.

3.2.2 Dynamic Focus Waveforms

The Waveform Generator outputs three horizontal rate waveforms; RH-FOCUS-PAR, GH-FOCUS-PAR, and BH-FOCUS-PAR. These waveforms are used by the FCM for dynamic focus correction of the red, green and blue CRTs, respectively. (Vertical dynamic focus waveforms are created by the VDM.)